# ML501 Evaluation Platform

## *User Guide*

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# Revision History

The following table shows the revision history for this document.

| Date | Version | Revision |
|---|---|---|
| 08/30/06 | 1.0 | Initial Xilinx release. |
| 09/18/06 | 1.0.1 | Minor typographical edit. |
| 03/15/07 | 1.1 | • Updated description for “4. Oscillator Sockets,” page 18<br>• Expanded Table 1-4, page 18<br>• Updated Appendix A, “Programming the IDT Clock Chip” |
| 11/26/07 | 1.2 | • Added sections on “MIG Compliance,” page 16 and “37. System Monitor,” page 34<br>• Added Appendix B, “References” |
| 06/13/08 | 1.2.1 | • Updated links in Appendix B, “References.”<br>• Removed obsolete reference to XAPP445. |
| 11/10/08 | 1.3 | • Added content to “17. System ACE and CompactFlash Connector,” page 27 and “Configuration Options,” page 36.<br>• Updated Platform Flash memory to Platform Flash PROM throughout. |
| 08/24/09 | 1.4 | • Updated the audio codec frequencyin “4. Oscillator Sockets.”<br>• Updated programming instructions for the Clock Generator in “Programming the IDT Clock Chip” in Appendix A. |

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# About This Guide

The ML50*x* evaluation platforms enable designers to investigate and experiment with features of Virtex®-5 FPGAs. This user guide describes the features and operation of the ML501 Evaluation Platform.

## Guide Contents

This manual contains the following chapters:

- Chapter 1, "ML501 Evaluation Platform," provides details on the board components
- Appendix A, "Programming the IDT Clock Chip," is a tutorial that steps through programming the clock chip on the ML501 board
- Appendix B, "References"

## Additional Documentation

The following documents are also available for download at http://www.xilinx.com/virtex5.

- Virtex-5 FPGA Family Overview

  The features and product selection of the Virtex-5 FPGA family are outlined in this overview.

- Virtex-5 FPGA Data Sheet: DC and Switching Characteristics

  This data sheet contains the DC and Switching Characteristic specifications for the Virtex-5 FPGA family.

- Virtex-5 FPGA User Guide

  This user guide includes chapters on:

  - Clocking Resources
  - Clock Management Technology (CMT)
  - Phase-Locked Loops (PLLs)
  - Block RAM and FIFO memory
  - Configurable Logic Blocks (CLBs)
  - SelectIO™ Resources
  - I/O Logic Resources
  - Advanced I/O Logic Resources

- Virtex-5 FPGA RocketIO GTP Transceiver User Guide

This guide describes the RocketIO™ GTP transceivers available in the Virtex-5 LXT and SXT platform devices.

- Virtex-5 FPGA Tri-Mode Ethernet Media Access Controller User Guide

  This user guide describes the dedicated Tri-Mode Ethernet Media Access Controller available in the Virtex-5 LXT and SXT platform devices.

- Virtex-5 FPGA Integrated Endpoint Block User Guide for PCI Express® Designs

  This user guide describes the integrated Endpoint blocks in the Virtex-5 LXT and SXT platform devices for PCI Express designs.

- XtremeDSP Design Considerations

  This guide describes the XtremeDSP. slice and includes reference designs for using the DSP48E.

- Virtex-5 FPGA Configuration User Guide

  This all-encompassing configuration guide includes chapters on configuration interfaces (serial and SelectMAP), bitstream encryption, Boundary-Scan and JTAG configuration, reconfiguration techniques, and readback through the SelectMAP and JTAG interfaces.

- Virtex-5 FPGA System Monitor User Guide

  The System Monitor functionality available in all the Virtex-5 devices is outlined in this guide.

- Virtex-5 FPGA Packaging and Pinout Specification

  This specification includes the tables for device/package combinations and maximum I/Os, pin definitions, pinout tables, pinout diagrams, mechanical drawings, and thermal specifications.

## Additional Support Resources

To search the database of silicon and software questions and answers, or to create a technical support case in WebCase, see the Xilinx® website at: http://www.xilinx.com/support.

## Typographical Conventions

This document uses the following typographical conventions. An example illustrates each convention.

| Convention | Meaning or Use | Example |
|---|---|---|
| *Italic font* | References to other documents | See the Virtex-5 *Configuration Guide* for more information. |
| | Emphasis in text | The address (F) is asserted *after* clock event 2. |
| Underlined Text | Indicates a link to a web page. | http://www.xilinx.com/virtex5 |

## Online Document

The following conventions are used in this document:

| Convention | Meaning or Use | Example |
|---|---|---|
| Blue text | Cross-reference link to a location in the current document | See the section "Additional Documentation" for details. |
| Red text | Cross-reference link to a location in another document | See Figure 5 in the *Virtex-5 Data Sheet* |
| Blue, underlined text | Hyperlink to a website (URL) | Go to http://www.xilinx.com for the latest documentation. |

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Chapter 1

# ML501 Evaluation Platform

## Introduction

The ML501 Evaluation Platform enables designers to investigate and experiment with features of Virtex-5 LX FPGAs. This user guide describes features and operation of the ML501 Evaluation Platform.

### Features

- Virtex-5 XC5VLX50-1FFG676 FPGA
- 64-bit DDR2 small outline DIMM (SODIMM), compatible with EDK supported IP and software drivers
- Programmable system clock generator chip
- One differential clock input pair and differential clock output pair with SMA connectors
- 3.3V clock oscillator socket populated with a 100-MHz oscillator
- General purpose DIP switches, LEDs, and pushbuttons
- Expansion header with 32 single-ended I/O, 16 LVDS capable differential pairs, 14 spare I/Os shared with buttons and LEDs, power, JTAG chain expansion capability, and IIC bus expansion
- Stereo AC97 audio codec with line-in, line-out, 50-mW headphone, microphone-in jacks, and SPDIF digital audio jacks
- RS-232 serial port
- 16-character x 2-line LCD display
- One 8-Kb IIC EEPROM
- DVI video connector (VGA supported with included adapter)
- PS/2 mouse and keyboard connectors
- System ACE™ CompactFlash configuration controller with Type I CompactFlash connector
- ZBT synchronous SRAM, 9 Mb on 32-bit data bus with four parity bits
- Intel P30 StrataFlash linear flash chips (32 MB)
- Serial Peripheral Interface™ (SPI) Flash (2 MB)
- 10/100/1000 tri-speed Ethernet PHY transceiver
- USB interface chip with host and peripheral ports
- Piezo audio transducer
- Rechargeable lithium battery to hold FPGA encryption keys

- Xilinx XC95144XL CPLD for glue logic
- Xilinx XCF32P Platform Flash PROM configuration storage device
- JTAG configuration port for use with Parallel Cable III, Parallel Cable IV, or Platform USB download cable
- Onboard power supplies for all necessary voltages
- Temperature and voltage monitoring chip with fan controller
- 5V @ 3A AC adapter
- Power indicator LED
- System monitor

## Package Contents

- Xilinx Virtex-5 FPGA ML501 Evaluation Platform
- System ACE CompactFlash card
- Power supply
- DVI to VGA adaptor

## Additional Information

For current information about the ML501 Evaluation Platform, visit www.xilinx.com/ml501

The information includes:

- Current version of this user guide in PDF format
- Example design files for demonstration of Virtex-5 FPGA features and technology
- Demonstration hardware and software configuration files for the System ACE controller, Platform Flash PROM configuration storage device, CPLD, and linear flash chips
- MicroBlaze™ EDK reference design files
- Full schematics in PDF format and ViewDraw schematic format
- PC board layout in Allegro PCB format
- Gerber files for the PC board (Many free or shareware Gerber file viewers are available on the internet for viewing and printing these files.)
- Additional documentation, errata, frequently asked questions, and the latest news

For information about the Virtex-5 family of FPGA devices, including product highlights, data sheets, user guides, and application notes, see the Virtex-5 FPGA website at www.xilinx.com/virtex5. Additional information is available from the data sheets and application notes from the component manufacturers.

## Block Diagram

Figure 1-1 shows a block diagram of the ML501 Evaluation Platform (board).

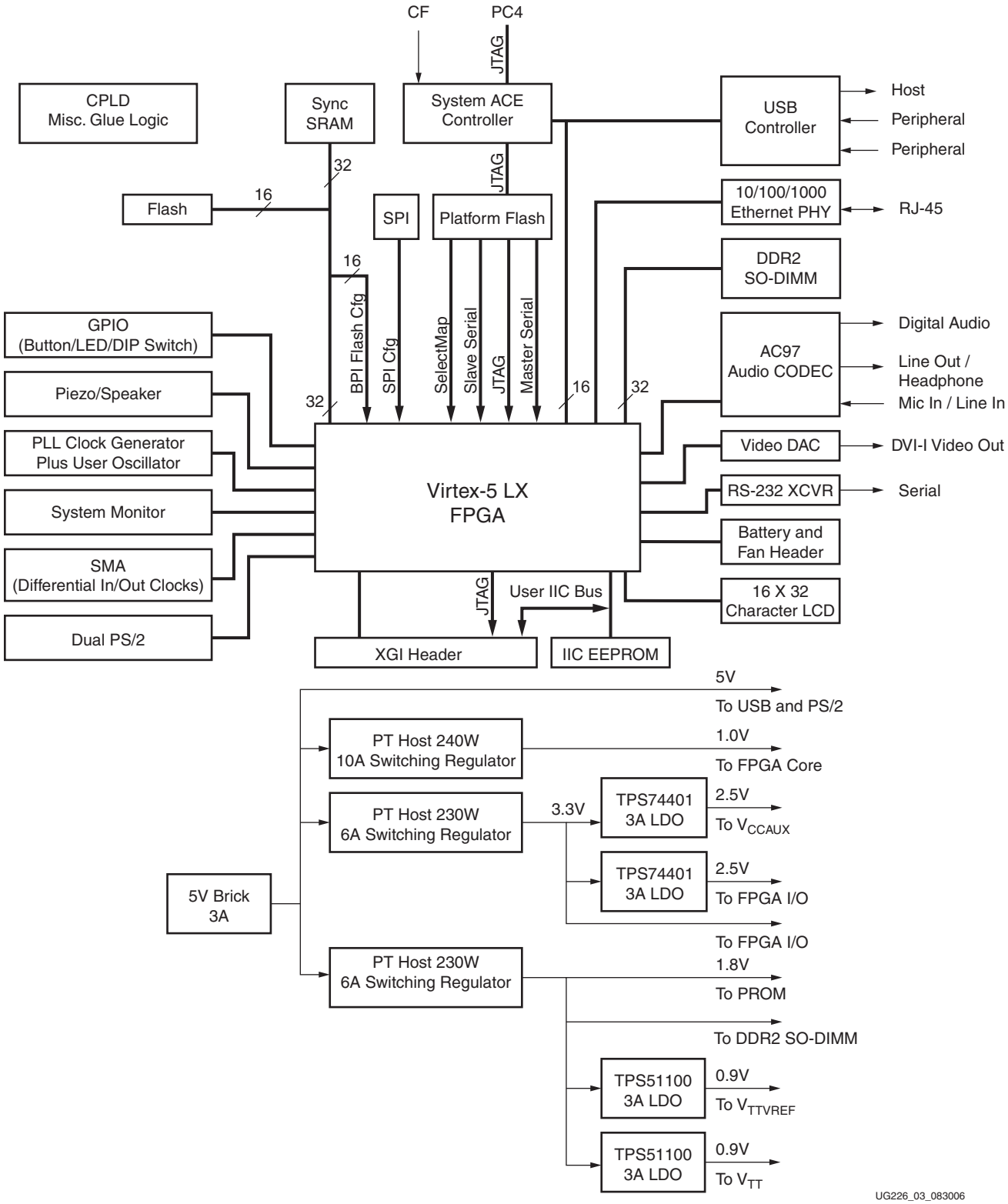


*Figure 1-1:* **Virtex-5 FPGA ML501 Evaluation Platform Block Diagram**

# Detailed Description

The ML501 Evaluation Platform (board) is shown in Figure 1-2 (front) and Figure 1-3, page 13 (back). The numbered sections on the pages following the figures contain details on each feature.

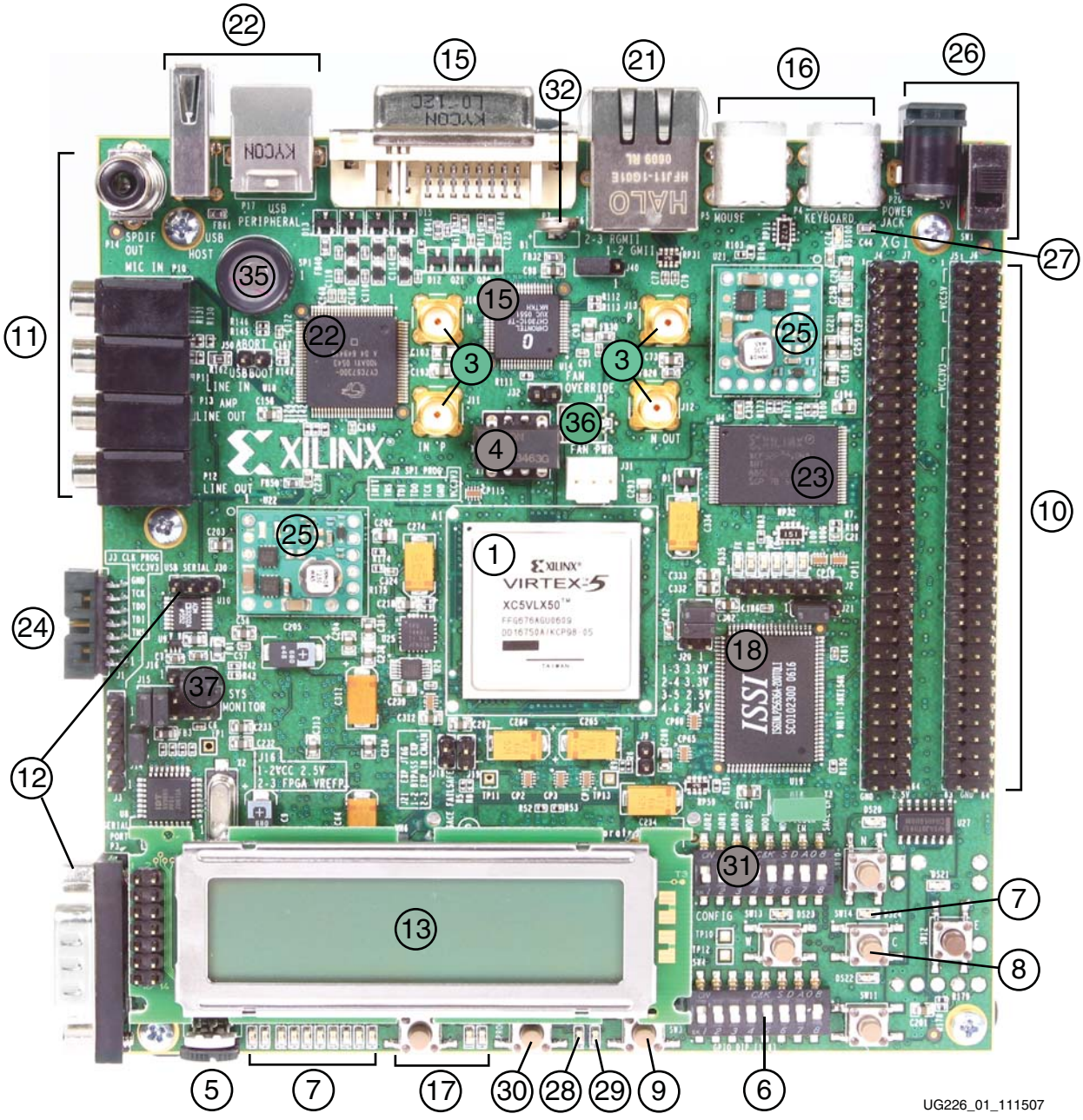


*Figure 1-2:* **Detailed Description of Virtex-5 FPGA ML501 Evaluation Platform Components (Front)**

***Note:*** The label on the CompactFlash (CF) card shipped with your board might differ from the one shown.

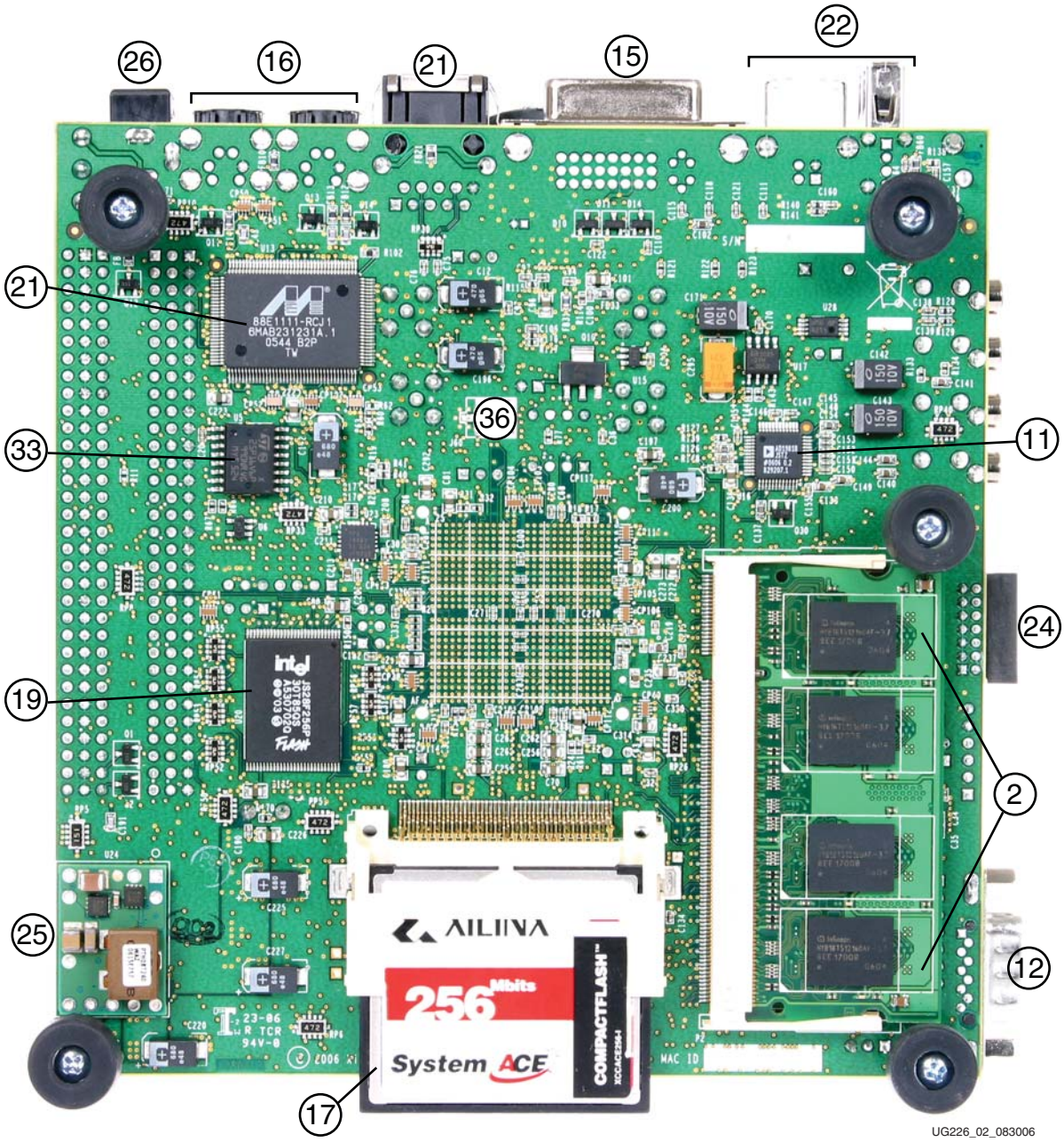


*Figure 1-3:* **Detailed Description of Virtex-5 FPGA ML501 Evaluation Platform Components (Back)**

# 1. Virtex-5 FPGA

A Xilinx Virtex-5 FPGA, XC5VLX50-1FFG676, is installed on the Evaluation Platform (the board).

## Configuration

The board supports configuration in all modes: JTAG, Master Serial, Slave Serial, Master SelectMAP, Slave SelectMAP, Byte-wide Peripheral Interface (BPI) Up, BPI Down, and SPI modes. See the "Configuration Options," page 36 section for more information.

## I/O Voltage Rails

The FPGA has 14 banks. The I/O voltage applied to each bank is summarized in Table 1-1.

*Table 1-1:* **I/O Voltage Rail of FPGA Banks**

| FPGA Bank | I/O Voltage Rail |
|---|---|
| 0 | 3.3V |
| 1 | 3.3V |
| 2 | 3.3V |
| 3 | 2.5V |
| 4 | 3.3V |
| 11 | User selectable as 2.5V or 3.3V using jumper J20 |
| 12 | 3.3V |
| 13 | User selectable as 2.5V or 3.3V using jumper J20 |
| 14 | 1.8V |
| 15 | 3.3V |
| 16 | 1.8V |
| 17 | 3.3V |
| 18 | 1.8V |
| 21 | 1.8V |

## Digitally Controlled Impedance

Some FPGA banks can support the digitally controlled impedance (DCI) feature in Virtex-5 FPGAs. Support for DCI is summarized in Table 1-2.

*Table 1-2:* **DCI Capability of FPGA Bank**

| FPGA Bank | DCI Capability |
|---|---|
| 1 | Not supported. |
| 2 | Not supported. |
| 3 | Not supported. |
| 4 | Not supported. |
| 11 | Yes, 49.9Ω resistors are installed. |
| 12 | Not supported. |
| 13 | Yes, 49.9Ω resistors are installed. |
| 14 | Yes, 49.9Ω resistors are installed. |
| 15 | Yes, 49.9Ω resistors are installed. |
| 16 | Yes, 49.9Ω resistors are installed. |
| 17 | Yes, 49.9Ω resistors are installed. |
| 18 | Not supported. |
| 21 | Yes, 49.9Ω resistors are installed. |

## 2. DDR2 SODIMM

The ML501 platform is shipped with a single-rank unregistered 256 MB SODIMM. The DDR2 SODIMM used is generally a Micron MT4HTF3264HY-53E or similar module. Serial Presence Detect (SPD) using an IIC interface to the DDR DIMM is also supported with the FPGA.

***Note:*** The board is only tested for DDR2 SDRAM operation at a 400 MHz data rate. Faster data rates might be possible but are not tested.

### MIG Compliance

The ML50*x* DDR2 interface is MIG pinout compliant. The MIG DDR2 routing guidelines outlined in the *Xilinx Memory Interface Generator (MIG) User Guide* [Ref 13] have been achieved.

The board's DDR2 SODIMM memory interface is designed to the requirements defined by the *MIG User Guide* using the MIG tool. The MIG documentation requires that designers follow the MIG pinout and layout guidelines. The MIG tool generates and ensures that the proper FPGA I/O pin selections are made in support of the board's DDR2 interface. The initial pin selection for the board was modified and then re-verified to meet the MIG pinout requirements. To ensure a robust interface, the ML50*x* DDR2 layout incorporates matched trace lengths for data signals to the corresponding data strobe signal as defined in the MIG user guide. See Appendix B, "References" for links to additional information about MIG and Virtex-5 FPGAs in general.

### DDR2 Memory Expansion

The DDR2 interface support user installation of SODIMM modules with more memory since higher order address and chip select signals are also routed from the SODIMM to the FPGA.

### DDR2 Clock Signal

Two matched length pairs of DDR2 clock signals are broadcast from the FPGA to the SODIMM. The FPGA design is responsible for driving both clock pairs with low skew. The delay on the clock trace is designed to match the delay of the other DDR2 control signals.

### DDR2 Signaling

All DDR2 SDRAM control signals are terminated through 47Ω resistors to a 0.9V VTT reference voltage. The FPGA DDR2 interface supports SSTL18 signaling and all DDR2 signals are controlled impedance. The DDR2 data, mask, and strobe signals are matched length within byte groups. The ODT functionality of the SODIMM should be utilized.

## 3. Differential Clock Input And Output With SMA Connectors

High-precision clock signals can be input to the FPGA using differential clock signals brought in through 50Ω SMA connectors. This allows an external function generator or other clock source to drive the differential clock inputs that directly feed the global clock input pins of the FPGA. The FPGA can be configured to present a 100Ω termination impedance.

A differential clock output from the FPGA is driven out through a second pair of SMA connectors. This allows the FPGA to drive a precision clock to an external device such as a piece of test equipment. Table 1-3 summarizes the differential SMA clock pin connections.

*Table 1-3:* **Differential SMA Clock Connections**

| Label | Clock Name | FPGA Pin |
|---|---|---|
| J10 | SMA_DIFF_CLK_IN_N | F10 |
| J11 | SMA_DIFF_CLK_IN_P | F9 |
| J12 | SMA_DIFF_CLK_OUT_N | F19 |
| J13 | SMA_DIFF_CLK_OUT_P | E18 |

## 4. Oscillator Sockets

The board has one crystal oscillator socket (X1) wired for standard LVTTL-type oscillators. It connects to the FPGA clock pin as shown in Table 1-4. The X1 socket is populated with a 100-MHz oscillator and is powered by the 3.3V supply.

The board also provides an IDT5V9885 (U8) EEPROM programmable clock generator device. This device is used to generate a variety of clocks to the board peripherals and FPGA. The programmable clock generator provides the following factory default single-ended outputs:

- 25 MHz to the Ethernet PHY (U13)
- 14.318 MHz to the audio codec (U16)
- 27 MHz to the USB controller (U18)
- 33 MHz to the Xilinx System ACE CF (U2)
- 33 MHz, 27 MHz, and a differential 200 MHz clock to the Xilinx FPGA

If users change the factory default configuration of the clock generator chip, the related reference design material might not work as designed. Instructions for returning the IDT5V9885 to the factory default configuration are provided in Appendix A, "Programming the IDT Clock Chip."

*Table 1-4:* **Oscillator Socket Connection**

| Label | Clock Name | FPGA Pin | Description |
|---|---|---|---|
| X1 | USER_CLK | AD8 | 100 MHz single-ended |
| U8 | CLK_33MHZ_FPGA | AB12 | 33 MHz single-ended |
| U8 | CLK_27MHZ_FPGA | AD13 | 27 MHz single-ended |
| U8 | CLK_DIFF_FPGA_P | E16 | 200 MHz differential pair (pos) |
| U8 | CLK_DIFF_FPGA_N | E17 | 200 MHz differential pair (neg) |

## 5. LCD Brightness and Contrast Adjustment

Turning potentiometer R87 adjusts the image contrast of the character LCD. The potentiometer should be turned with a screwdriver.

## 6. DIP Switches (Active-High)

Eight general-purpose (active-High) DIP switches are connected to the user I/O pins of the FPGA. Table 1-5 summarizes these connections.

*Table 1-5:* **DIP Switch Connections (SW4)**

| SW4 | FPGA Pin |
|---|---|
| GPIO_DIP_SW1 | U4 |
| GPIO_DIP_SW2 | V3 |
| GPIO_DIP_SW3 | T4 |
| GPIO_DIP_SW4 | T5 |
| GPIO_DIP_SW5 | U6 |

*Table 1-5:* **DIP Switch Connections (SW4) *(Continued)***

| SW4 | FPGA Pin |
|---|---|
| GPIO_DIP_SW6 | U5 |
| GPIO_DIP_SW7 | U7 |
| GPIO_DIP_SW8 | T7 |

## 7. User and Error LEDs (Active-High)

There are a total of 15 active-High LEDs directly controllable by the FPGA:

- Eight green LEDs are general purpose LEDs arranged in a row
- Five green LEDs are positioned next to the North-East-South-West-Center-oriented pushbuttons (only the *center* one is cited in Figure 1-2, page 12)
- Two red LEDs are intended to be used for signaling error conditions, such as bus errors, but can be used for any other purpose

Some LEDs are buffered through the CPLD to allow the LED signals to be used as higher-performance I/O by way of the XGI expansion connector. Table 1-6 summarizes the LED definitions and connections.

*Table 1-6:* **User and Error LED Connections**

| Reference Designator | Label/Definition | Color | FPGA Pin | Buffered |
|---|---|---|---|---|
| DS20 | LED North | Green | Y8 | Yes |
| DS21 | LED East | Green | Y18 | Yes |
| DS22 | LED South | Green | AA8 | Yes |
| DS23 | LED West | Green | AA18 | Yes |
| DS24 | LED Center | Green | T22 | Yes |
| DS17 | GPIO LED 0 | Green | E13 | Yes |
| DS16 | GPIO LED 1 | Green | D14 | Yes |
| DS15 | GPIO LED 2 | Green | E12 | Yes |
| DS14 | GPIO LED 3 | Green | F12 | Yes |
| DS13 | GPIO LED 4 | Green | D15 | No |
| DS12 | GPIO LED 5 | Green | E15 | No |
| DS11 | GPIO LED 6 | Green | E10 | No |
| DS10 | GPIO LED 7 | Green | E11 | No |
| D56 | Error 1 | Red | N4 | No |
| D55 | Error 2 | Red | P5 | No |

## 8. User Pushbuttons (Active-High)

Five active-High user pushbuttons are available for general purpose usage and are arranged in a North-East-South-West-Center orientation (only the *center* one is cited in Figure 1-2, page 12). Table 1-7 summarizes the user pushbutton connections.

*Table 1-7:* **User Pushbutton Connections**

| Reference Designator | Label/Definition | FPGA Pin |
|---|---|---|
| SW10 | N (GPIO North) | A22 |
| SW12 | E (GPIO East) | A23 |
| SW11 | S (GPIO South) | B22 |
| SW13 | W (GPIO West) | C21 |
| SW14 | C (GPIO Center) | B21 |

## 9. CPU Reset Button (Active-Low)

The CPU reset button is an active-Low pushbutton and is used as a system or user reset button. This pushbutton switch is wired only to an FPGA I/O pin so it can also be used as a general-purpose pushbutton switch (see Table 1-8).

*Table 1-8:* **CPU Reset Connections**

| Reference Designator | Label/Definition | FPGA Pin |
|---|---|---|
| SW3 | CPU RESET | T23 |

## 10. XGI Expansion Headers

The board contains expansion headers for easy expansion or adaptation of the board for other applications. The expansion connectors use standard 0.1-inch headers. The expansion connectors contain connections to single-ended and differential FPGA I/Os, ground, 2.5V/3.3V/5V power, JTAG chain, and the IIC bus. All signals on connectors J4 and J6 have matched length traces that are matched to each other.

### Differential Expansion I/O Connectors

Header J4 contains 16 pairs of differential signal connections to the FPGA I/Os. This permits the signals on this connector to carry high-speed differential signals, such as LVDS data. All differential signals are routed with 100Ω differential trace impedance. Matched length traces are used across all differential signals on J4. Consequently, these signals connect to the FPGA I/O, and they can be used as independent single-ended nets. The $V_{CCIO}$ of these signals can be set to 2.5V or 3.3V by setting jumper J20. Table 1-9, page 21 summarizes the differential connections on this expansion I/O connector.

*Table 1-9:* **Expansion I/O Differential Connections (J4)**

| J4 Differential Pin Pair | | Schematic Net Name | | FPGA Pin | |
|---|---|---|---|---|---|
| **Pos** | **Neg** | **Pos** | **Neg** | **Pos** | **Neg** |
| 4 | 2 | HDR2_4 | HDR2_2 | F24 | F25 |
| 8 | 6 | HDR2_8 | HDR2_6 | E25 | E26 |
| 12 | 10 | HDR2_12 | HDR2_10 | G21 | G22 |
| 16 | 14 | HDR2_16 | HDR2_14 | P19 | N19 |
| 20 | 18 | HDR2_20 | HDR2_18 | J25 | J26 |
| 24 | 22 | HDR2_24 | HDR2_22 | R22 | R23 |
| 28 | 26 | HDR2_28 | HDR2_26 | N22 | N21 |
| 32 | 30 | HDR2_32 | HDR2_30 | V26 | U26 |
| 36 | 34 | HDR2_36 | HDR2_34 | K23 | K22 |
| 40 | 38 | HDR2_40 | HDR2_38 | G26 | H26 |
| 44 | 42 | HDR2_44 | HDR2_42 | L20 | L19 |
| 48 | 46 | HDR2_48 | HDR2_46 | P23 | N23 |
| 52 | 50 | HDR2_52 | HDR2_50 | G24 | G25 |
| 56 | 54 | HDR2_56 | HDR2_54 | M20 | M19 |
| 60 | 58 | HDR2_60 | HDR2_58 | H24 | J24 |
| 64 | 62 | HDR2_64 | HDR2_62 | P21 | P20 |

## Single-Ended Expansion I/O Connectors

Header J6 contains 32 single-ended signal connections to the FPGA I/Os. This permits the signals on this connector to carry high-speed, single-ended data. All single-ended signals on connector J6 are matched length traces. The $V_{CCIO}$ of these signals can be set to 2.5V or 3.3V by setting jumper J20. Table 1-10 summarizes the single-ended connections on this expansion I/O connector.

*Table 1-10:* **Expansion I/O Single-Ended Connections (J6)**

| J6 Pin | Schematic Net Name | FPGA Pin |
|---|---|---|
| 2 | HDR1_2 | J20 |
| 4 | HDR1_4 | J23 |
| 6 | HDR1_6 | J21 |
| 8 | HDR1_8 | H23 |
| 10 | HDR1_10 | M22 |
| 12 | HDR1_12 | K20 |
| 14 | HDR1_14 | K21 |
| 16 | HDR1_16 | M21 |
| 18 | HDR1_18 | L25 |
| 20 | HDR1_20 | L24 |
| 22 | HDR1_22 | K26 |
| 24 | HDR1_24 | K25 |
| 26 | HDR1_26 | M26 |
| 28 | HDR1_28 | M25 |
| 30 | HDR1_30 | N24 |
| 32 | HDR1_32 | M24 |
| 34 | HDR1_34 | AB25 |
| 36 | HDR1_36 | N26 |
| 38 | HDR1_38 | P25 |
| 40 | HDR1_40 | P24 |
| 42 | HDR1_42 | T24 |
| 44 | HDR1_44 | T25 |
| 46 | HDR1_46 | U24 |
| 48 | HDR1_48 | U25 |
| 50 | HDR1_50 | W25 |
| 52 | HDR1_52 | W26 |
| 54 | HDR1_54 | Y25 |

*Table 1-10:* **Expansion I/O Single-Ended Connections (J6) *(Continued)***

| J6 Pin | Schematic Net Name | FPGA Pin |
|---|---|---|
| 56 | HDR1_56 | Y26 |
| 58 | HDR1_58 | P26 |
| 60 | HDR1_60 | AA25 |
| 62 | HDR1_62 | AC26 |
| 64 | HDR1_64 | AB26 |

## Other Expansion I/O Connectors

In addition to the high-speed I/O paths, additional I/O signals and power connections are available to support expansion cards plugged into the ML501 board. Fourteen I/O pins from the general-purpose pushbutton switches and LEDs on the board are connected to expansion connector J5. This permits additional I/Os to connect to the expansion connector if the pushbutton switches and LEDs are not used. The connection also allows the expansion card to utilize the pushbutton switches and LEDs on the board.

The expansion connector also allows the board's JTAG chain to be extended onto the expansion card by setting jumper J21 accordingly.

The IIC bus on the board is also extended onto the expansion connector to allow additional IIC devices to be bused together. If the expansion IIC bus is to be utilized, the user must have the IIC pull-up resistors present on the expansion card. Bidirectional level shifting transistors allow the expansion card to utilize 2.5V to 5V signaling on the IIC bus.

Power supply connections to the expansion connectors provide ground, 2.5V, 3.3V, and 5V power pins. If the expansion card draws significant power from the ML501 board, ensure that the total power draw can be supplied by the board.

The ML501 expansion connector is backward compatible with the expansion connectors on the ML40*x*, ML32*x*, and ML42*x* boards, thereby allowing their daughter cards to be used with the ML501 Evaluation Platform. Table 1-11, page 24 summarizes the additional expansion I/O connections.

*Table 1-11:* **Additional Expansion I/O Connections (J5)**

| J5 Pin | Label | FPGA Pin | Description |
|---|---|---|---|
| 1 | VCC5 | – | 5V Power Supply |
| 2 | VCC5 | – | 5V Power Supply |
| 3 | VCC5 | – | 5V Power Supply |
| 4 | VCC5 | – | 5V Power Supply |
| 5 | NC | – | Not Connected |
| 6 | VCC3V3 | – | 3.3V Power Supply |
| 7 | VCC3V3 | – | 3.3V Power Supply |
| 8 | VCC3V3 | – | 3.3V Power Supply |
| 9 | VCC3V3 | – | 3.3V Power Supply |
| 10 | NC | – | Not Connected |
| 11 | FPGA_EXP_TMS | – | Expansion TMS |
| 12 | FPGA_EXP_TCK | – | Expansion TCK |
| 13 | FPGA_EXP_TDO | – | Expansion TDO |
| 14 | FPGA_EXP_TDI | – | Expansion TDI |
| 15 | GPIO_LED_N | Y8 | LED North |
| 16 | SW3 (N) | A22 | GPIO Switch North |
| 17 | GPIO_LED_C | T22 | LED Center |
| 18 | SW14 (C) | B21 | GPIO Switch Center |
| 19 | GPIO_LED_W | AA18 | LED West |
| 20 | SW13 (W) | C21 | GPIO Switch West |
| 21 | GPIO_LED_S | AA8 | LED South |
| 22 | SW11 (S) | B22 | GPIO Switch South |
| 23 | GPIO_LED_E | Y18 | LED East |
| 24 | SW12 (E) | A23 | GPIO Switch East |
| 25 | GPIOLED 0 | E13 | GPIO LED 0 |
| 26 | GPIOLED 1 | D14 | GPIO LED 1 |
| 27 | GPIOLED 2 | E12 | GPIO LED 2 |
| 28 | GPIOLED 3 | F12 | GPIO LED 3 |
| 29 | NC | - | Not Connected |
| 30 | NC | - | Not Connected |
| 31 | IIC_SCL_EXP | R20 | Expansion IIC SCL |
| 32 | IIC_SDA_EXP | T20 | Expansion IIC SDA |

## 11. Stereo AC97 Audio Codec

The ML501 board has an AC97 audio codec (U16) to permit audio processing. The Analog Devices AD1981 Audio Codec supports stereo 16-bit audio with up to 48-kHz sampling. The sampling rate for record and playback can be different.

***Note:*** The reset for the AC97 codec is shared with the reset signal for the flash memory chips and is designed to be asserted at power-on or at system reset.

Separate audio jacks are provided for Microphone, Line In, Line Out, and Headphone. All jacks are stereo except for Microphone. The Headphone jack is driven by the audio codec's internal 50-mW amplifier. The SPDIF jack supplies digital audio output from the codec. Table 1-12 summarizes the audio jacks.

*Table 1-12:* **ML501 Audio Jacks**

| Reference Designator | Function |
|---|---|
| P10 | Microphone - In |
| P11 | Analog Line - In |
| P12 | Analog Line - Out |
| P13 | Headphone - Out |
| P14 | SPDIF - Out |

## 12. RS-232 Serial Port

The ML501 board contains one male DB-9 RS-232 serial port, allowing the FPGA to communicate serial data with another device. The serial port is wired as a host (DCE) device. Therefore, a null modem cable is normally required to connect the board to the serial port on a computer. The serial port is designed to operate up to 115200 Bd. An interface chip is used to shift the voltage level between FPGA and RS-232 signals.

***Note:*** The FPGA is connected only to the TX and RX data pins on the serial port. Therefore, other RS-232 signals, including hardware flow-control signals, are not used. Flow control should be disabled when communicating with a computer.

A secondary serial interface is available by using header J30 to support debug of the USB controller chip. Header J30 brings out RS-232 voltage level signals for ground, TX data, and RX data.

## 13. 16-Character x 2-Line LCD

The ML501 board has a 16-character x 2-line LCD (Tianma TM162VBA6) on the board to display text information. Potentiometer R87 adjusts the contrast of the LCD. The data interface to the LCD is connected to the FPGA to support 4-bit mode only. The CPLD is used to shift the voltage level between the FPGA and the LCD. The LCD module has a connector that allows the LCD to be removed from the board to access to the components below it.

***Caution!*** Care should be taken not to scratch or damage the surface of the LCD window.

## 14. IIC Bus with 8-Kb EEPROM

An IIC EEPROM (STMicroelectronics M24C08) is provided on the board to store non-volatile data such as an Ethernet MAC address. The EEPROM is located under the removable LCD and is not visible in Figure 1-2. The EEPROM write protect is disabled on the board. IIC bus pull-up resistors are provided on the board.

The IIC bus is extended to the expansion connector so that the user can add additional IIC devices and share the IIC controller in the FPGA. If the expansion IIC bus is to be utilized, the user must have additional IIC pull-up resistors present on the expansion card. Bidirectional level shifting transistors allow the expansion card to utilize 2.5V to 5V signaling on IIC.

## 15. DVI Connector

A DVI connector (P7) is present on the board to support an external video monitor. The DVI circuitry utilizes a Chrontel CH7301C capable of 1600 X 1200 resolution with 24-bit color. The video interface chip drives both the digital and analog signals to the DVI connector. A DVI monitor can be connected to the board directly. A VGA monitor can also be connected to the board using the supplied DVI-to-VGA adaptor. The Chrontel CH7301C is controlled by way of the VGA IIC bus.

The DVI connector supports the IIC protocol to allow the board to read the monitor's configuration parameters. These parameters can be read by the FPGA using the VGA IIC bus.

## 16. PS/2 Mouse and Keyboard Ports

The ML501 Evaluation Platform contains two PS/2 ports: one for a mouse (P5) and the other for a keyboard (P4). Bidirectional level shifting transistors allow the FPGA's 1.8V I/O to interface with the 5V I/O of the PS/2 ports. The PS/2 ports on the board are powered directly by the main 5V power jack, which also powers the rest of the board.

***Caution!*** Care must be taken to ensure that the power load of any attached PS/2 devices does not overload the AC adapter.

## 17. System ACE and CompactFlash Connector

The Xilinx System ACE CompactFlash (CF) configuration controller allows a Type I CompactFlash card to program the FPGA through the JTAG port. Both hardware and software data can be downloaded through the JTAG port. The System ACE controller supports up to eight configuration images on a single CompactFlash card. The configuration address switches allow the user to choose which of the eight configuration images to use.

The CompactFlash card shipped with the board is correctly formatted to enable the System ACE CF controller to access the data stored in the card. The System ACE CF controller requires a FAT16 file system, with only one reserved sector permitted, and a sector-per-cluster size of more than one (UnitSize greater than 512). The FAT16 file system supports partitions of up to 2 GB. If multiple partitions are used, the System ACE directory structure must reside in the first partition on the CompactFlash, with the `xilinx.sys` file located in the root directory. The `xilinx.sys` file is used by the System ACE CF controller to define the project directory structure, which consists of one main folder containing 8 sub-folders used to store the 8 ACE files containing the configuration images. Only one ACE file should exist within each sub-folder. All folder names must be compliant to the DOS 8.3 short filename format. This means that the folder names can be up to eight characters long, and cannot contain the following reserved characters: `< > " / \ |`. This DOS 8.3 filename restriction does not apply to the actual ACE file names. Other folders and files may also coexist with the System ACE CF project within the FAT16 partition. However, the root directory must not contain more than a total of 16 folder and/or file entries, including deleted entries.

When ejecting or unplugging the CompactFlash device, it is important to safely stop any read or write access to the CompactFlash device to avoid data corruption. If the CompactFlash file system becomes corrupted, a copy of the original demonstration image (as shipped with the board), as well as instructions for re-imaging the CompactFlash card to restore the original demonstration image are available online. See *CompactFlash Re-Imaging Instructions* at http://www.xilinx.com/products/boards/ml501/images.htm.

Within the demonstration image, *Configuration Image 6 (cfg6) My Own ACE File* is reserved as a placeholder to be replaced by a user design. After creating a new ACE file, the ACE file can be copied from your computer to the ML50*x*\cfg6 directory on the CompactFlash card using a CompactFlash programmer (USB CompactFlash reader/writer devices or PC card adapters are available at computer stores). For step-by-step instructions on how to create a new ACE file from an FPGA bitstream (and ELF file) using XMD and the `genace.tcl` script, See the *My Own ACE File* section in the *ML501 Getting Started Tutorial* [Ref 10] as well as the *Stand-Alone Software Applications* section in the *ML501 Reference Design User Guide* [Ref 11].

System ACE error and status LEDs indicate the operational state of the System ACE controller:

- A blinking red error LED indicates that no CompactFlash card is present
- A solid red error LED indicates an error condition during configuration
- A blinking green status LED indicates a configuration operation is ongoing
- A solid green status LED indicates a successful download

Every time a CompactFlash card is inserted into the System ACE socket, a configuration operation is initiated. Pressing the System ACE reset button re-programs the FPGA.

***Note:*** System ACE configuration is enabled by way of a DIP switch. See "31. Configuration Address and Mode DIP Switches."

The board also features a System ACE *failsafe* mode. In this mode, if the System ACE controller detects a failed configuration attempt, it automatically reboots back to a predefined configuration image. The failsafe mode is enabled by inserting two jumpers across J18 and J19 (in horizontal or vertical orientation).

***Caution!*** Use caution when inserting a CompactFlash card with exposed metallic surfaces. Improper insertion can cause a short with the traces or components on the board.

The System ACE MPU port is connected to the FPGA. This connection allows the FPGA to use the System ACE controller to reconfigure the system or access the CompactFlash card as a generic FAT file system. The data bus for the System ACE MPU port is shared with the USB controller.

## 18. ZBT Synchronous SRAM

The ZBT synchronous SRAM (ISSI IS61NLP25636A-200TQL) provides high-speed, low-latency external memory to the FPGA. The memory is organized as 256K x 36 bits. This organization provides for a 32-bit data bus with support for four parity bits.

***Note:*** The SRAM and FLASH memory share the same data bus.

## 19. Linear Flash Chips

A NOR linear flash device (Intel JS28F256P30T95) is installed on the board to provide 32 MB of flash memory. This memory provides non-volatile storage of data, software, or bitstreams. The flash chip is 16 bits wide and shares its data bus with SRAM. The flash memory can also be used to program the FPGA.

***Note:*** The reset for the AC97 Codec is shared with the reset signal for the flash memory chips and is designed to be asserted at power-on or at system reset.

## 20. Xilinx XC95144XL CPLD

A Xilinx XC95144XL CPLD provides general-purpose glue logic for the board. The CPLD is located under the removable LCD and is not visible in Figure 1-2. The CPLD is programmed from the main JTAG chain of the board. The CPLD is mainly used to implement level translators, simple gates, and buffers.

## 21. 10/100/1000 Tri-Speed Ethernet PHY

The ML501 Evaluation Platform contains a Marvell Alaska PHY device (88E1111) operating at 10/100/1000 Mb/s. The board supports MII, GMII, and RGMII interface modes with the FPGA. The PHY is connected to a Halo HFJ11-1G01E RJ-45 connector with built-in magnetics. The PHY is configured to default at power-on or reset to the following

settings (See Table 1-13). These settings can be overwritten via software. Jumper J40 selects whether the PHY defaults to RGMII mode (pin 2-3) or GMII mode (pin 1-2).

*Table 1-13:* **Board Connections for PHY Configuration Pins**

| Config Pin | Connection on Board | Bit[2] Definition and Value | Bit[1] Definition and Value | Bit[0] Definition and Value |
|---|---|---|---|---|
| CONFIG0 | $V_{CC}$ 2.5V | PHYADR[2] = 1 | PHYADR[1] = 1 | PHYADR[0] = 1 |
| CONFIG1 | Ground | ENA_PAUSE = 0 | PHYADR[4] = 0 | PHYADR[3] = 0 |
| CONFIG2 | $V_{CC}$ 2.5V | ANEG[3] = 1 | ANEG[2] = 1 | ANEG[1] = 1 |
| CONFIG3 | $V_{CC}$ 2.5V | ANEG[0] = 1 | ENA_XC = 1 | DIS_125 = 1 |
| CONFIG4 | $V_{CC}$ 2.5V or LED_DUPLEX (Set by J40) | HWCFG_MODE[2] = 0 or 1 (Set by J40) | HWCFG_MODE[1] = 1 | HWCFG_MODE[0] = 1 |
| CONFIG5 | $V_{CC}$ 2.5V | DIS_FC = 1 | DIS_SLEEP = 1 | HWCFG_MODE[3] = 1 |
| CONFIG6 | LED_RX | SEL_BDT = 0 | INT_POL = 1 | 75/50Ω = 0 |

## 22. USB Controller with Host and Peripheral Ports

A Cypress CY7C67300 embedded USB host controller provides USB connectivity for the board. The USB controller supports host and peripheral modes of operation. The USB controller has two serial interface engines (SIE) that can be used independently. SIE1 is connected to the USB Host connector (P19). SIE2 is connected only to the USB Peripheral connector (P17).

The USB controller has an internal microprocessor to assist in processing USB commands. The firmware for this processor can be stored in its own dedicated IIC EEPROM (U28) or can be downloaded from a host computer via a peripheral connector. The USB controller's serial port is connected to J30 through an RS-232 transceiver to assist with debug. Jumper J50 can be installed to prevent the USB controller from executing firmware stored in the IIC EEPROM.

## 23. Xilinx XCF32P Platform Flash PROM Configuration Storage Device

Xilinx XCF32P Platform Flash PROM configuration storage device offers a convenient and easy-to-use configuration solution for the FPGA. The Platform Flash PROM holds up to two separate configuration images (up to four with compression) that can be accessed through the configuration address switches. To use the Platform Flash PROM to configure the FPGA, the configuration DIP switch must be set to the correct position.

The Platform Flash PROM can program the FPGA by using the master or slave configuration in serial or parallel (SelectMap) modes. The Platform Flash PROM is programmed using Xilinx iMPACT software through the board's JTAG chain. See the "Configuration Options," page 36 section for more information.

## 24. JTAG Configuration Port

The JTAG configuration port for the board (J1) allows for device programming and FPGA debug. The JTAG port supports the Xilinx Parallel Cable III, Parallel Cable IV, or Platform USB cable products. Third-party configuration products might also be available. The JTAG chain can also be extended to an expansion board by setting jumper J21 accordingly. See the "Configuration Options," page 36 section for more information.

## 25. Onboard Power Supplies

Power supply circuitry on the board generates 0.9V, 1.0V, 1.8V, 2.5V, and 3.3V voltages to power the components on the board. The 1.0V, 1.8V, and 3.3V supplies are driven by Texas Instruments PTH08T2 switching power regulators. These regulators are driven with a 400 kHz clock so they run synchronous to each other, reducing noise caused by beat frequencies. The clocks sent to each regulator are also out of phase to reduce reflected noise at the input. In addition, the board utilizes the regulators' *turbo trans* feature to improve output transient response.

The diagram in Figure 1-4 shows the power supply architecture and maximum current handling on each supply. The typical operating currents are significantly below the maximum capable. The ML501 board is normally shipped with a 15W power supply, which should be sufficient for most applications.

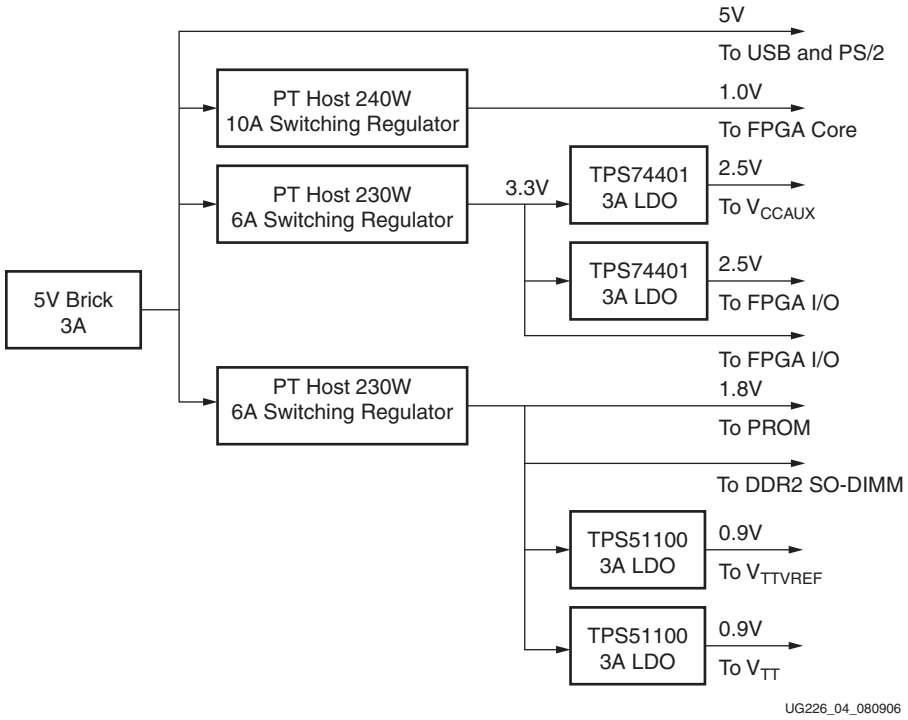


*Figure 1-4:* **Power Supply Diagram**

## 26. AC Adapter and Input Power Switch/Jack

The ML501 board ships with a 15W (5V @ 3A) AC adapter. The power connector is a 2.1 mm x 5.5 mm barrel type plug (center positive). For applications requiring additional power, such as the use of expansion cards drawing significant power, a larger AC adapter might be required. If a different AC adapter is used, its load regulation should be less than 10% or better than ±10%. The power switch turns the board on and off by controlling the 5V supply to the board

## 27. Power Indicator LED

The PWR Good LED lights when the 5V supply is applied.

## 28. INIT LED

The INIT LED lights upon power-up to indicate that the FPGA has successfully powered up and completed its internal power-on process.

## 29. DONE LED

The DONE LED indicates the status of the DONE pin on the FPGA. It should be lighted when the FPGA is successfully configured.

## 30. Program Switch

This switch grounds the FPGA's **Prog** pin when pressed. This action clears the FPGA.

## 31. Configuration Address and Mode DIP Switches

The 8-position DIP switch (SW15) sets the address and mode of configuration. It also enables fallback configuration of the Platform Flash PROM and enables System ACE configuration. Table 1-14 lists the function of each switch.

*Table 1-14:* **Configuration Address DIP Switch Settings**

| Switch (SW15) | Function |
|---|---|
| 1 | Config Address [2]. |
| 2 | Config Address [1]. |
| 3 | Config Address [0]. |
| 4 | MODE [2]. |
| 5 | MODE [1]. |
| 6 | MODE [0]. |
| 7 | Platform Flash PROM Fallback (On = Enable, Off = Disable).(1) |
| 8 | System ACE Configuration (On = Enable, Off = Disable). When enabled, the System ACE controller configures the FPGA from the CF card whenever a card is inserted or the SYSACE RESET button is pressed. |

**Notes:**

1. Reserved for future use. Not currently implemented.

Configuration Address [2:0] allows the user to select among multiple configuration images. For System ACE configuration, up to eight possible configurations can be stored on a CF card. The Platform Flash PROM and Linear Flash can hold up to four separate bitstreams that can be chosen by Configuration Address [2:0].

Mode[2:0] selects the FPGA configuration mode according to Table 1-15.

*Table 1-15:* **Configuration Mode DIP Switch Settings**

| Mode[2:0] | Mode |
|---|---|
| 000 | Master Serial (Platform Flash PROM, up to four configurations) |
| 001 | SPI (One configuration) |
| 010 | BPI Up (Parallel NOR Flash, up to four configurations) |
| 011 | BPI Down (Parallel NOR Flash, up to four configurations) |
| 100 | Master SelectMAP (Platform Flash PROM, up to four configurations) |
| 101 | JTAG (PC4, System ACE up to eight configurations) |
| 110 | Slave SelectMAP (Platform Flash PROM, up to four configurations) |
| 111 | Slave Serial (Platform Flash PROM, up to four configurations) |

## 32. Encryption Key Battery

An onboard rechargeable lithium battery is connected to the $V_{BATT}$ pin of the FPGA to hold the encryption key for the FPGA.

## 33. SPI Flash

The ML501 board has a 16-Mb SPI Flash (ST Microelectronics M25P16). The SPI Flash can be used for FPGA configuration or to hold user data. The SPI Flash can be in-system programmed using a Xilinx download cable.

## 34. IIC Fan Controller and Temperature/Voltage Monitor

Onboard temperature and voltage monitoring and control is handled by an Analog Devices ADT7476A chip. This chip is controlled via IIC and can provide the following functions:

- Measure the voltage of 5V, 3.3V, 1.8V, and 1.0V supplies
- Measure FPGA temperature via DXP/DXN pins on the FPGA
- Measure ambient temperature
- Read power good status signals from 2.5V linear regulators
- PWM control of fan speed
- Fan Tachometer readings
- Generate interrupts/alarms based on readings

Connector J31 is a keyed three-pin fan header similar to those found in computers. It is designed to support a 5V DC fan. To bypass the fan controller chip and operate the fan at full speed, the user can populate connector J32.

For high-power operating conditions, a heatsink and/or fan for the FPGA can be accommodated on the board. The ML501 does not ship with a heatsink/fan unit but can accommodate one (for example, Calgreg Electronics Smart-CLIP family of heatsink/fan assemblies).

## 35. Piezo

A piezo audio transducer is provided to allow simple beeps, tones, and songs to be played. The piezo is driven by a transistor controlled by the FPGA.

## 36. FMC Connectors for Power Supply Analysis

The FMC connector (Rosenberger 16P101-40M L4) is a small, form-factor, surface mount, 50Ω coaxial connector suitable for high-frequency signal analysis.

The board has a pair of FMC connectors attached to 1.0V power supply. This permits the user to perform spectrum analysis of the behavior of the power supply during board operation. This can help the user tune the power supply decoupling network for optimal performance. Because two FMC connectors are attached to the same power supply (on opposite sides of the board), the user can use one FMC connector to inject a high frequency signal into the power plane while the second FMC is connected to test equipment that measures the response of the board.

By default, the FMC connectors are not soldered on. Contact Rosenberger of North America (www.rosenbergerna.com) to order the FMC connector. Rosenberger also manufactures adapter cables that allow SMA-based test equipment or cables to be connected to the FMC connectors.

***Note:*** Xilinx is not responsible for damage caused by a user attempting to solder the FMC connectors onto the board.

## 37. System Monitor

The ML501 supports both the dedicated and the auxiliary analog inputs to the Virtex-5 FPGA System Monitor block. The VP and VN pins shown in Table 1-16, page 34 are the dedicated pins, whereas the VAUXP[*x*], VAUXN[*x*] represent the 16 user-selectable auxiliary analog input channels. The ML501 PCB layout for the VP and VN pins is designed using differential pairs and anti-alias filtering in close proximity to the FPGA as recommended in the *Virtex-5 FPGA System Monitor User Guide* [Ref 8]. Please note that the circuitry connected to the 16 AUX channels on the ML501 are connected in a non-optimal fashion as they are implemented without anti-alias filtering at the FPGA. This tradeoff was made as the AUX channels are also used as general-purpose I/O on the XGI connectors (see "10. XGI Expansion Headers," page 20 for additional details). The AUX channels are still available for use with the System Monitor functions, but they will not attain the performance level of the dedicated analog input as noted in the *Virtex-5 FPGA System Monitor User Guide*. Access to the dedicated analog input pairs (VP/VN) is provided through pins 9 and 10 of the System Monitor Header (J15). See Table 1-16.

The Virtex-5 FPGA System Monitor function is built around a 10-bit, 200-kSPS (kilosamples per second) Analog-to-Digital Converter (ADC). When combined with a number of on-chip sensors, the ADC is used to measure FPGA physical operating parameters like on-chip power supply voltages and die temperatures. Access to external voltages is provided through a dedicated analog-input pair (VP/VN) and 16 user selectable analog inputs, known as auxiliary analog inputs (VAUXP[15:0], VAUXN[15:0]).

The System Monitor is fully functional on power up, and measurement data can be accessed via the JTAG port pre-configuration. The Xilinx ChipScope™ Pro tool provides access to the System Monitor over the JTAG port. The System Monitor control logic implements some common monitoring features. For example, an automatic channel sequencer allows a user-defined selection of parameters to be automatically monitored, and user-programmable averaging is enabled to ensure robust noise-free measurements.

The System Monitor also provides user-programmable alarm thresholds for the on-chip sensors. Thus, if an on-chip monitored parameter moves outside the user-specified operating range, an alarm logic output becomes active. In addition to monitoring the on-chip temperature for user-defined applications, the System Monitor issues a special alarm called Over-Temperature (OT) if the FPGA temperature becomes critical (> 125°C). The over-temperature signal is deactivated when the device temperature falls below a user-specified lower limit. If the FPGA power-down feature is enabled, the FPGA enters power down when the OT signal becomes active. The FPGA powers up again when the alarm is deactivated.

For additional information about the System Monitor, see http://www.xilinx.com/systemmonitor and consult the *Virtex-5 FPGA System Monitor User Guide* [Ref 8]. Table 1-16 shows the System Monitor connections.

*Table 1-16:* **System Monitor Connections**

| External Input | FPGA Pin | Header Pin | Schematic Net Name |
|---|---|---|---|
| VN | P13 | J15-10 | FPGA_V_N |
| VP | N14 | J15-9 | FPGA_V_P |
| VAUXN[0] | N24 | J6-30 | HDR1_30_SM_0_N |
| VAUXP[0] | M24 | J6-32 | HDR1_32_SM_0_P |
| VAUXN[1] | M26 | J6-26 | HDR1_26_SM_1_N |

*Table 1-16:* **System Monitor Connections *(Continued)***

| External Input | FPGA Pin | Header Pin | Schematic Net Name |
|---|---|---|---|
| VAUXP[1] | M25 | J6-28 | HDR1_28_SM_1_P |
| VAUXN[2] | K26 | J6-22 | HDR1_22_SM_2_N |
| VAUXP[2] | K25 | J6-24 | HDR1_24_SM_2_P |
| VAUXN[3] | L25 | J6-18 | HDR1_18_SM_3_N |
| VAUXP[3] | L24 | J6-20 | HDR1_20_SM_3_P |
| VAUXN[4] | J24 | J4-58 | HDR2_58_SM_4_N |
| VAUXP[4] | H24 | J4-60 | HDR2_60_SM_4_P |
| VAUXN[5] | G25 | J4-50 | HDR2_50_SM_5_P |
| VAUXP[5] | G24 | J4-52 | HDR2_52_SM_5_P |
| VAUXN[6] | H26 | J4-38 | HDR2_38_SM_6_N |
| VAUXP[6] | G26 | J4-40 | HDR2_40_SM_6_P |
| VAUXN[7] | E26 | J4-6 | HDR2_6_SM_7_N |
| VAUXP[7] | E25 | J4-8 | HDR2_8_SM_7_P |
| VAUXN[8] | F25 | J4-2 | HDR2_2_SM_8_N |
| VAUXP[8] | F24 | J4-4 | HDR2_4_SM_8_P |
| VAUXN[9] | P20 | J4-62 | HDR2_62_SM_9_N |
| VAUXP[9] | P21 | J4-64 | HDR2_64_SM_9_P |
| VAUXN[10] | R23 | J4-22 | HDR2_22_SM_10_N |
| VAUXP[10] | R22 | J4-22 | HDR2_24_SM_10_P |
| VAUXN[11] | N21 | J4-26 | HDR2_26_SM_11_N |
| VAUXP[11] | N22 | J4-28 | HDR2_28_SM_11_P |
| VAUXN[12] | N23 | J4-46 | HDR2_46_SM_12_N |
| VAUXP[12] | P23 | J4-48 | HDR2_48_SM_12_P |
| VAUXN[13] | M19 | J4-54 | HDR2_54_SM_13_N |
| VAUXP[13] | M20 | J4-56 | HDR2_56_SM_13_P |
| VAUXN[14] | L19 | J4-42 | HDR2_42_SM_14_N |
| VAUXP[14] | L20 | J4-44 | HDR2_44_SM_14_P |
| VAUXN[15] | K22 | J4-34 | HDR2_34_SM_15_N |
| VAUXP[15] | K23 | J4-36 | HDR2_36_SM_15_P |

# Configuration Options

The FPGA on the ML501 Evaluation Platform can be configured by five major devices:

- Xilinx download cable (JTAG)
- System ACE controller (JTAG)
- Platform Flash PROM
- Linear Flash memory
- SPI Flash memory

The following section provides an overview of the possible ways the FPGA can be configured.

## JTAG (Xilinx Download Cable and System ACE Controller) Configuration

The FPGA, Platform Flash PROM, and CPLD can be configured through the JTAG port. The JTAG chain of the board is illustrated in Figure 1-5.

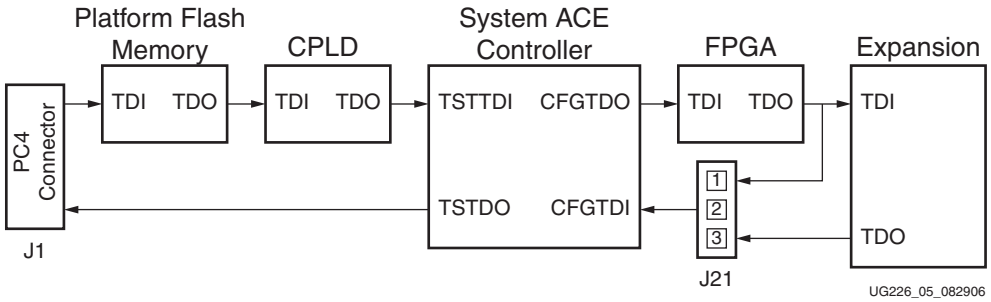


*Figure 1-5:* **JTAG Chain**

The chain starts at the PC4 connector and goes through the System ACE controller, the Platform Flash PROM, the FPGA, the CPLD, and an optional extension of the chain to the expansion card. Jumper J21 determines if the JTAG chain should be extended to the expansion card.

The JTAG chain can be used to program the FPGA and access the FPGA for hardware and software debug. The JTAG chain is also used to program the Platform Flash PROM and the CPLD.

The PC4 JTAG connection to the JTAG chain allows a host computer to download bitstreams to the FPGA using the iMPACT software tool. PC4 also allows debug tools such as the ChipScope™ Pro Analyzer or a software debugger to access the FPGA.

The System ACE controller can also program the FPGA through the JTAG port. Using an inserted CompactFlash card, configuration information can be stored and played out to the FPGA. The System ACE controller supports up to eight configuration images that can selected using the three configuration address DIP switches. Under FPGA control, the System ACE chip can be instructed to reconfigure to any of the eight configuration images.

The configuration mode should be set to `101`. Jumper J21 should exclude the expansion card from the JTAG chain, and switch SW15, pin 8 should be ON to use System ACE configuration. When set correctly, the System ACE controller programs the FPGA upon power-up if a CompactFlash card is present or whenever a CompactFlash card is inserted. Pressing the System ACE reset button also causes the System ACE controller to program the FPGA if a CompactFlash card is present.

## Platform Flash PROM Configuration

The Platform Flash PROM can also be used to program the FPGA. The Platform Flash PROM can hold up to two configuration images (up to four with compression), which are selectable by the two least significant bits of the configuration address DIP switches.

The board is wired so the Platform Flash PROM can download bitstreams in Master Serial, Slave Serial, Master SelectMAP (parallel), or Slave SelectMAP (parallel) modes. Using the iMPACT tool to program the Platform Flash PROM, the user has the option to select which of the four modes to use for programming the FPGA. The configuration mode DIP switches on the board must be set to match the programming method being used by the Platform Flash PROM.

When set correctly, the Platform Flash PROM programs the FPGA upon power-up or whenever the **Prog** button is pressed.

## Linear Flash Memory Configuration

Data stored in the linear flash can be used to program the FPGA (BPI mode). Up to four configuration images can theoretically be supported.

The configuration mode DIP switches on the board must be set to `010` for BPI_up or `011` for BPI_down.

When set correctly, the FPGA is programmed upon power-up or whenever the **Prog** button is pressed.

## SPI Flash Memory Configuration

Data stored in SPI can be used to program the FPGA. The configuration mode DIP switches must be set to `001` for SPI configuration.

When set correctly, the FPGA is programmed upon power-up or whenever the **Prog** button is pressed.

Appendix A

# Programming the IDT Clock Chip

## Overview

ML50*x* evaluation boards feature an Integrated Device Technology (IDT) 3.3V EEPROM Programmable Clock Generator that is pre-programmed at the factory. In the event the chip programming is changed, the instructions in this appendix show how to return the clock chip to its factory default settings using the following equipment:

- Xilinx download cable
- JTAG flying wires

## Downloading to the ML50*x* Board

1. Connect a Xilinx download cable to the board using flying leads connected to jumper J3 (Figure A-1).

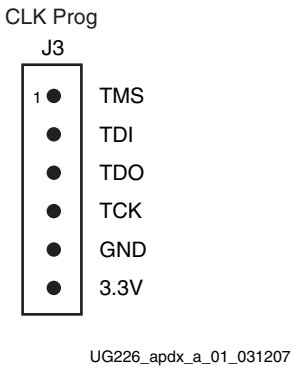


*Figure A-1:* **J3 IDT5V9885 JTAG Connector**

2. Set a jumper across J14 to enable JTAG programming of the IDT clock chip.
3. Click **Start** → **iMPACT**.
4. Click Boundary Scan.
5. Right-click **Add Xilinx Device…**
6. Locate the SVF file (`ML50X_clock_setup.svf` in the example shown in Figure A-2, page 40) and click **Open**.

   ***Note:*** The `ML50X_clock_setup.svf` file is available on the ML50*x* product page.
7. Right-click on the device and select **Execute XSVF/SVF**.

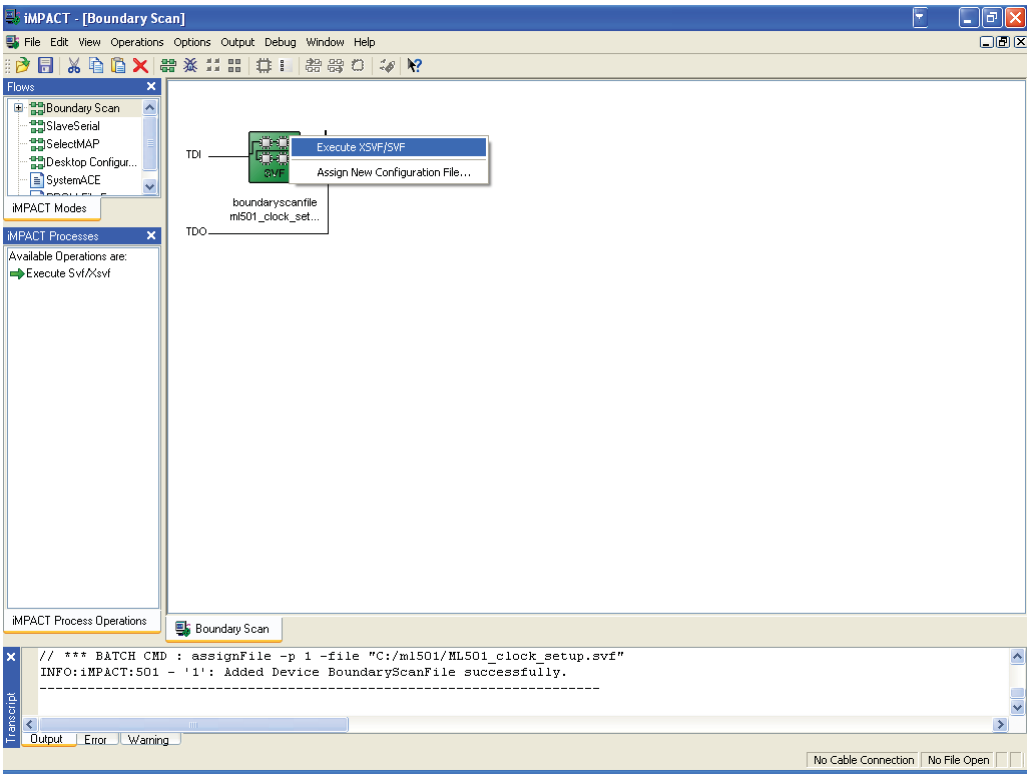


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*Figure A-2:* **Programming the IDT5V9885 on the ML50*x* Using iMPACT**

8. To finish programming the chip, cycle the power by turning off the board power switch.
9. After turning the board back on, verify that the clock frequencies are correct.

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Appendix B

# References

Documents supporting Virtex-5 FPGAs:

1. DS100, *Virtex-5 FPGA Family Overview.*
2. DS202, *Virtex-5 FPGA Data Sheet: DC and Switching Characteristics.*
3. UG190, *Virtex-5 FPGA User Guide.*
4. UG194, *Virtex-5 FPGA Tri-Mode Ethernet Media Access Controller User Guide.*
5. UG197, *Virtex-5 FPGA Integrated Endpoint Block User Guide for PCI Express Designs.*
6. UG193, *XtremeDSP Design Considerations.*
7. UG191, *Virtex-5 FPGA Configuration User Guide.*
8. UG192, *Virtex-5 FPGA System Monitor User Guide.*
9. UG195, *Virtex-5 FPGA Packaging and Pinout Specification.*

Documents specific to the ML501 Evaluation Platform:

10. UG228, *ML501 Getting Started Tutorial.*
11. UG227, *ML501 Reference Design User Guide.*

The Xilinx Memory Solutions Web page offers the following material supporting the Memory Interface Generator (MIG) tool:

12. WP260, *Memory Interfaces Made Easy with Xilinx FPGAs and the Memory Interface Generator.*
13. UG086, *Xilinx Memory Interface Generator (MIG) User Guide* (for registered users).
14. Demos on Demand, *Memory Interface Solutions with Xilinx FPGAs.*
15. Xilinx Support - Memory Interface Resources (for registered users).